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10/627,269	07/25/2003	Hong-Yi Hubert Chen	MP0357	7592

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/627,269	CHEN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 26 July 2006.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-74 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-74 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                     | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 26, 2006 has been entered.
2. Claims 1, 8, 10, 14, 21, 23, 27, 29, 38, 40, 49, 56-57, 65 and 67-69 are amended and claim 13 added again. Therefore, claims 1-74 are pending in the application.

***Terminal Disclaimer***

3. The terminal disclaimer filed on July 26, 2006 disclaiming the terminal portion of any patent granted on this application, which would extend beyond the expiration date of any patent granted on Application Number 10/666,892 has been reviewed and is accepted. The terminal disclaimer has been recorded. Accordingly, the double patenting rejection made in the previous office action has been withdrawn.
4. Applicant's arguments filed on July 26, 2006 have been fully considered but they are not deemed to be persuasive.
5. The rejection of claims 1-74 as in the previous Office Action is respectfully maintained and reiterated below for Applicant's convenience.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-18, 21-26 and 49-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaggar (USPN: 5,701,493).

As per claim 1, Jaggar teaches a register file for a data processing system comprising an unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8).

As per claim 2, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register

(i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claim 3, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 4, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the input ports (i.e. the “reg add”, mode bits input to 17 and input to 8 in Fig. 8) receive at least one source register index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 5, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further comprising an address encoder (i.e. the combination of components 12-20 in Fig. 8) to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 8, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more instructions being processed is outputted from the unbanked memory unit (i.e. the MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 9, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further comprising input ports (i.e. the “reg add”, mode bits input to 17 and input to 8 in Fig. 8) to receive at least one write index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for writing data to at least one register (i.e. to R0-R15 in Fig. 8); and at least one write input port (i.e. input port to the read buffer 8 shown in Fig. 8) for writing the data to the register (i.e. R0-R15 in Fig. 8) addressable by the encoded address (e.g. see Fig. 8).

As per claim 10, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more executed instructions (i.e. instructions/commands buffered in instruction register 12 in Fig. 8) for the data processing are written into the unbanked memory unit (i.e. MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 11, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 12, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claims 14-18 and 21-25, see arguments with respect to the rejection of claims 1-5 and 8-12, respectively. Claims 14-18 and 21-25 are also rejected based on the same rationale as the rejection of claims 1-5 and 8-12, respectively.

As per claims 13 and 26, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claim 49, Jaggar teaches a microprocessor comprising an integrated circuit comprising a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); and at least one address encoder (i.e. the combination of components 12-20 in Fig. 8) to provide at least one encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for addressing at least one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see the abstract and Figs. 1 and 8).

As per claims 50-53 and 55, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 50-53 and 55 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 54, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that at least one input (i.e. the “reg add”, mode bits input to

17 and input to 8 in Fig. 8) to receive index (i.e. the register address input) and processor mode information (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8); and at least one output (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data stored in the storage location (i.e. from the register) addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 56, Jaggar teaches a data processing system comprising a memory mapped register file for accessing a plurality of registers (i.e. memory locations) using an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode) (e.g. see the abstract and the Figs. 1 and 8).

As per claims 57 and 63, see arguments with respect to the rejection of claims 49 and 54, respectively. Claims 57 and 63 are also rejected based on the same rationale as the rejection of claims 49 and 54, respectively.

As per claims 58-62 and 64, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 58-62 and 64 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 65, Jaggar teaches an integrated circuit method comprising configuring the integrated circuit to receive processor mode (i.e. a user mode and

system mode) and source data inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8); configuring the integrated circuit to determine an encoded address based on the processor mode and source data inputs, wherein the encoded address corresponds to a respective one of a plurality of registers (i.e. memory locations) and a corresponding processor mode (i.e. a user mode and system mode); configuring the integrated circuit to address one of the registers using an encoded address; and configuring the integrated circuit to output data from the register addressable by the encoded address (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) (e.g. see the abstract and Figs. 1 and 8).

As per claim 66, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to output data for multiple instructions (i.e. via the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8).

As per claim 67, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers addressable by an encoded address (e.g. see the abstract).

As per claim 68, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers for multiple executed instructions (i.e. via the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8).

As per claims 69-74, see arguments with respect to the rejection of claims 1, 65, 65 and 66-68, respectively. Claims 69-74 are also rejected based on the same rationale as the rejection of claims 1, 65, 65 and 66-68, respectively.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6-7 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Meier et al. (USPN: 6,363,471) hereinafter, Meier.

As per claims 6 and 7, Jaggar teaches the claimed invention as described above, but failed to teach a latch circuit and a selector as claimed. Meier, however, teaches about using the latch or other clocked storage devices to store the intermediate values for pipelining to the next stage (e.g. see Col. 16, lines 21-35 and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Meier's latch circuit in the register file taught by Jaggar. In doing so, this latch circuit can buffer the data (i.e. the encoded addresses) for pipeline storage in case if the data can be reused. The further limitation of having the selector coupled to the latch and the address encoder is well-known and notorious old in the art at the time of the current invention was made. By using the selector, such

as a mux, the encoded address can be selected either from the latch circuit or directly from the address encoder based on a select signal.

As per claims 19-20, see arguments with respect to the rejection of claims 6-7, respectively. Claims 19-20 are also rejected based on the same rationale as the rejection of claims 6-7, respectively.

8. Claims 27-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Kerr et al. (USPN: 2003/0159021) hereinafter, Kerr.

As per claim 27, Jaggar teaches a data processing system comprising a microprocessor (i.e. 62 in Fig. 8) comprising a register file, the register file including a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8).

However, Jaggar does not teach that the microprocessor comprising a plurality of pipeline stages. Kerr, on the other hand, teaches the microprocessor (i.e. the TMC

core, 600 in Fig. 6) comprising a plurality of pipeline stages (i.e. 610, 620, 630 and 660 in Fig. 6) (e.g. see paragraph [0003] and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the plurality of pipeline stages taught by Kerr in the data processing system of Jaggar. In doing so, a number of instructions are being executed in parallel and as a result of that the overall performance of the data processing system increases.

As per claim 28, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claims 29, 31 and 32, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Kerr teaches that the pipeline stages include an instruction fetch stage (i.e. IF 610 in Fig. 6) to fetch one or more instructions; an instruction decode stage (i.e. ID 620 in Fig. 6) to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the memory unit (i.e. 640 in Fig. 6) for outputting data from or writing data to one or more of the registers (i.e. 652, 654 in Fig. 6), an execution stage (i.e. EX 630 in Fig. 6) including a plurality of execution units (i.e. 646 and 656 in Fig. 6), each execution unit to receive data from the register file for executing an instruction, and a write back or retire logic stage (i.e. WB 660 in Fig. 6) to receive results data associated with one or

more instructions executed by the execution units of the execution stage, and to forward the results data to the register file for storage (i.e. via bus 426 in Fig. 6) (e.g. see Fig. 6 and paragraphs [0038]-[0040]).

As per claim 30, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs from the instruction decode stage, the inputs being used to obtain the encoded address for accessing at least one register; and at least one output port (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from the register addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 33 the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive the data from the write back or retire logic for one or more executed instructions, the data to be written in the register file (e.g. see Figs. 1 and 8).

As per claim 34, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs.

1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 35, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 36, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claim 37, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claims 38-48, see arguments with respect to the rejection of claims 27-37, respectively. Claims 38-48 are also rejected based on the same rationale as the rejection of claims 27-37, respectively.

### ***Remarks***

9. As to the remark, Applicant asserted that with regards to independent claims 1 and 27,

- (a) Jaggar fails to show, teach or suggest a register file for a data processing system comprising an unbanked memory unit having a plurality of registers addressable by an encoded address. Instead, as best understood by Applicants, Jaggar discloses a banked register structure.
- (b) Jaggar fails to disclose the limitation of an unbanked memory unit having a plurality of registers addressable by an encoded address.
- (c) Jaggar is absent of any teaching or suggestion of an unbanked memory unit that includes a plurality of registers addressable by encoded addresses, and instead is directed to a banked architecture that accesses banked registers in separate memory units.
- (d) Figs. 2 and 9 of Jaggar disclose the banked memory architecture. Fig. 9 appears to disclose different banks of registers for User32, System, FIQ32, SVC32, Abt32, IRQ32 and Undef32 modes.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a)-(d), Examiner first would like to point out to Applicant that according to paragraphs [003]-[007] of the specification of the current application, broadly, the “banked” general purpose registers means there are one or more registers specified for use in specific processing mode; and the “unbanked” general purpose registers means all registers are usable for different processing modes based on the processing mode encoded in the address. In Jaggar prior art, all (0000-1111) registers are usable based on processing mode selected by the mode bits. Therefore, Jaggar prior art does teach the unbanked memory unit (i.e. the stack memory area having 0000-1111 registers/memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8). Fig. 9 of the Jaggar prior art shows that all 16 registers are usable/available for all modes (i.e. the user mode and exception modes) it is different from the Fig. 1 of the current application because only specific (not all) registers are usable for a given processing mode.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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